Response to the Pre-bid queries of the RFP for deployment linked incentive for design, development, manufacture, validation and deployment of two types of secure systems on chips (SoCs) using Indian owned processor based on open source

Tender Reference # MeitY/SoC/DLI/01/2022-2023 dated 07th September 2022

Company Name	S.No.	Pre-bid Query/ RFP Section	Pre-bid Query	Response
Powai Labs	**1**	**Can one make different SoC, based on the user requirements?**		As mentioned in the Section 6(e) (i.e. **Minimum Indicated Broad Specifications**) in Synopsis of the RFP, while bidders are free to arrive at the optimum design/ configuration/ layout/ architecture of the SoCs to meet the market requirements and to enhance their marketability, it is mandatory for the SoCs to meet the Minimum Indicated Broad Specifications and features mentioned in the RFP. Bidders are free to include additional features and functionalities to meet the chosen applications and end user's requirements. If the bidder wishes to develop variants of BSC-1 & BSC-2 to optimize the utility on more applications, they may do so as long as they don't dilute the Minimum Indicated Broad Specifications, as mentioned in the RFP.

HCL	**1**	**How will Defence ministry accept product from private industry, is there any list of products that Defence ministry will publish for using these min 50,000 products (10% of 5Lakhs units). Will we have a accelerated end user acceptance for these defence products, as we have only 2.25years only for the overall design-prototype-demonstrate-user acceptance-volume deployment cycle (which is very small for a defence product development cycle).**		Please refer Para 4d. Point I (Page 24) of RFP which states - The Bidder shall produce production grade SoCs and undertake validation of ICD and testing of the protocols required for specific application/ specified by the equipment manufacturer/ end user. The Bidder is expected to independently interact with prospective product manufacturer and draw out testing and validation requirements and satisfy them. However, for 10% mandatory deployment in defence & aerospace, MoD may consider mandating utilisation of indigenous SoCs, post suitable testing/ validation/ certification. DPSU like BEL could also be encouraged to engage in joint production & marketing. The O/o ADG Acq-Tech (M&S), MoD will be the Single Point of Contact in MoD for any further interaction on the case.
	2	**Is the requirement of 22nm/28nm process mandatory ?**		As mentioned at Appendix-E (i.e. MINIMUM INDICATED BROAD SPECIFICATIONS FOR BSC-1& BSC-2 SoCs) of the RFP, the suggested CMOS Technology node for ASIC implementation is 22nm/ 28nm. However, the bidder may choose other process(es) as deemed appropriate to the application(s) selected by the bidder.

	3	**Is there any other requirement like how many years the product is to be sold in the market ?**		As mentioned in the Section 5(g) & 5(h) (i.e. Period Scheme and Warranty Period) in Synopsis of the RFP, deployment of designated number of each SoCs in next two years @ 25% every 6 months. While the bidder may choose so, the RFP doesn't mandate any requirement of selling product in market Post-Contract period.
	4	**How long Is the Silicon owners expected to maintain the RoT certificates after sale of devices ?**		As mentioned in the Section 6(e) (i.e. Financial Aspects) in Synopsis of the RFP, the bidder should independently carry out the process of verification, testing and validation for satisfying the end users for deployment in their respective systems and provide necessary documentation to MeitY Committee to review and verify the eligibility for release of the DLI amount. While Silicon owners may chose to maintain the RoT certificates after sale of devices as per the requirements of the end user, the RFP doesn't mandate any such condition other than listed above.

Cyhub Technologies Private Ltd	**1**	**Has the power consumption of indian designed processors been benchmarked.**		As per the Scope of work of the RFP, Selected Bidder shall identify a suitable 64-bit Indian owned processor based on Open Source ISA and check its stability & suitability to design and develop the SoCs. The SoCs has to meet the minimum indicated broad specifications mentioned at Appendix-E in RFP. The Selected Bidder shall have to submit a report on stability & suitability of core and that it meets the minimum specifications of the SoCs and the requirement of prospective deployment in the identified applications. In other words, the onus of selecting the India owned processor based on Open-Source ISA and checking its stability & suitability lies with the bidder; which should appropriately meet the minimum indicated broad specifications of BSC-1 and BSC-2.
	2	**Will the list of available designs be vetted and released by MeitY for reference**		
	3	**Has EMI/EMC benchmarking for reference processors been done.**		
	4	**For Cyber Security: will MeitY provide subsidy for training human resource for peripheral development since they can be used across the industry to further design indigenously**		As per RFP. No additional subsidy and tax exemption envisaged at present in the RFP.

	5	**Will tax exemption be provided under 80 D For Cyber Security: since it is strategic R&D**		
Dyumnin Semiconductors	**1**	**From the RFQ it is not clear whether the requirement is for: 1. Physical design and tapeout of an already designed SoC**		As per the Scope of work of the RFP, the selected Bidder shall identify a suitable 32-bit or 64-bit Indian owned processor based on Open Source ISA, check its stability & suitability and design, develop, manufacture, Validate, deploy and provide warranty support for designated number of SoCs (5 lakhs) of BSC-1 & BSC-2 SoCs. Accordingly, the bidder may choose any of the listed requirements in the query (#1 or #2) as deemed appropriate to the bidder to implement the scope of work of RFP.
	2	**2. RTL Design of IP('s) + SOC as per requirement using Shakti-code as the Processor, followed by the physical design process.**		
		If it is #2 my company will be interested in bidding for this.		

Shakra Innovations Pvt. Ltd.	**1**	**We understand that the successful bidder is expected to develop and deploy end-user products in both defence and non-defence domains. In order to meet the deadline durations given, it would be much required for a SPOC from the Defence ministry or organizations to work with the successful bidder from T0 (start) for the successful identification of a minimum of 6 Defence products that will be able to use BSC1 and BSC2 and provide an accelerated user acceptance for us to meet the timeline of deploying these devices within the four years' timeline. We would anticipate that the technical compliance work to the requirements should start IN PARALLEL and along with finalising the end deployment use case scenarios for the given timeline to be met**		For 10% mandatory deployment in defence & aerospace, MoD may consider mandating utilisation of indigenous SoCs, post suitable testing/ validation/ certification. DPSU like BEL could also be encouraged to engage in joint production & marketing. The O/o ADG Acq-Tech (M&S), MoD will be the Single Point of Contact in MoD for any further interaction on the case.

	2	**Will the MeitY / Defence ministry provide a mandate for compulsory use of BSC1 and BSC2 for all Government support programs like the Smart City, EB meter etc once Silicon is available in the open market (~ 2 years from T0) ? This is to facilitate the bid and deploy the 5 lakh silicon as a complete product.**		RFP doesn't mandate the compulsory use of BSC1 and BSC2 for Government support programs. In the current RFP, there is no provision for Preferential Market Access for the devices. However, for 10% mandatory deployment in defence & aerospace, MoD may consider mandating utilisation of indigenous SoCs, post suitable testing/ validation/ certification.DPSU like BEL could also be encouraged to engage in joint production & marketing. The O/o ADG Acq-Tech (M&S), MoD will be the Single Point of Contact in MoD for any further interaction on the case.
	3	**Since there's not many companies for high volume OSAT in India, will MeitY relax the packaging to be done in India condition for the successful bidder? We can have the Security programming done in India and as-and-when we have OSAT in India, we can move to those OSATs to manufacture the devices.**		This will be reveiewed on case to case basis and a waiver may be provided.
Kalatronics Semiconductors Private Limited	**1**	**Referring to: MINIMUM INDICATED BROAD SPECIFICATIONS FOR BSC-1 SoC. CPU CORES Category: L2 Cache / TCM. Is it LI cache/ TCM if not please clarify why L2 Cache is equated with TCM?**		Provide a second level memory structure after the L1 to improve performance. This memory structure can either be an L2 or TCM or both (dynamic reconfiguration). Either one of the three options are valid interpretations.

	2	**CPU Extensions: Category Floating point operators. Is this required to be IEEE 754-2008 compliant or equivalent such as POSIT. What is the precision required viz., half, full, double, quadruple precisions.**		FPU to be IEEE 754-2008 compliant. Precision required may be decided by the applications targeted. For POSIT Artmhemntic may be based on end user requirement.
	3	**MINIMUM INDICATED BROAD SPECIFICATIONS FOR BSC-1 SoC: Category : Security TAMPER DETECTION. Please define the expectations of TAMPER DETECTION**		An input signal to the SoC may be added; which may initiate a guaranteed fail safe secure shutdown of the device, leaving no scope for any data leakage.
	4	**ADC/DAC — Is this 12/ 16 bits the accuracy or resolution that you desire**		Resolution
	5	**For BSC2-2: 1. For camera interface is there any standard interface preferred?**		MIPI-CSI or any other standard interface as per the application required.
	6	**We would like to understand more on PSIMD**		While the PSIMD (Packed Single Instruction Multiple Data) definition is inspired from RISC-V, the RFP expectation is to provide a vector unit for DSP like applications.

	7	**All across the document the phrase "checking stability and suitability" of the Indian owned microprocessor keeps surfacing. We want to have clarification on this because we don't want (See page 18j Schedule of Work & Timelines Point I to become an issue**		The onus of selecting the India owned processor based on Open-Source ISA and checking its stability & suitability lies with the bidder; which should appropriately meet the minimum indicated broad specifications of BSC-1 and BSC-2.

	8	**However, it seems to be fundamental objections to using "shuttles" - See for example (Page 28) Point 5 (e). This seems to indicate that EVERY chip being manufactured MUST be traceable. Does this apply to prototyping phase? If yes, then shuttles and other shared vehicles are a challenge. It certainly applies to production and maintaining this database for every chip means that every chip will need to havea unique serial number - only on package or also on the die? In the latter it will be another use of efuse and we need to dice and package in-house and then assign serial numbers to all dies (in-house) and under some agreed-upon process destroy the bad chips. Also see (page 30) Point 12(a): The "Process Security" mentions some business process standard but can safely guess that shuttle runs will fail it. Also see (page 3! j Point 12(c): An ARM specific standard is referred as a compliance requirement. Not very sure if all details are available in the public domain? Also see page 40) Point 23(c): So the "secure" business process applies to the design phase too**		Database for Deployment is for uniquely identifying and tracing the manufactured chips and their deployment for disbursing incentives. The security requirement are essential as per the RFP.

	9	**Appendix E— BSC-1 requirement: (a) We need to know about the sampling rate of the ADC and / or the desired bandwidths of the 8 analog channels; ditto for the DAC (b) You mention a Temp Monitor: is this for on-die temp measurement or external temp measurement? What range of temperatures? Contact or non-contact measurement - any requirement?**		Sampling rate/bandwidth may be decided based on the application. Temp monitor is for SoC on-die temp. mesaurement. Temp. range can be -40 to 150 degree celsius.
Mindgrove Technologies Pvt. Ltd.	**1**	**RFP Page #- Section- Sub-section: 16 – 2 (d) (i): Checking stability & suitability of Indian processor core:**	**What is envisaged in the Stability Check phase? Some of the existing Indian-owned processors (such as Shakti and Vega) have already been taped out and have been demonstrated in the field. Would this contribute to the Stability Check? Are there any criteria that have been envisaged in this stage?**	As per Section 4(a) of Scope of work in the RFP (i.e. **Stage-I: Checking Suitability of Indian Processor & Submission of Project Report**), Bidder shall select a **32-bit or 64-bit Indian Owned Processor based on Open Source ISA** (designed in India) and undertake necessary checks to ascertain its stability & suitability for the stated SoCs and submit its report. In other words, the onus lies with the bidder in respect of selecting the appropriate processor (which may be a 3rd party IP) and checking its stability & suitability to design and develop the SoCs; which should meet the minimum indicated broad specifications of BSC-1 and BSC-2. RFP doesn't mandate any specific criteria other than listed above.

	2	**RFP Page #- Section- Sub-section: 6 – 4: Broad Description of the Task and Deliverables. In addition to design, the development and packaging has to be in India by Indian entity:**	**There are no ATMP providers in India, at least capable of handling BGA packaging (which is what both BSC-1 and BSC-2 will require), though there are projects ongoing to setup such units. If such services capable of handling the advanced packaging that this project requires are not available, this would breach the condition that "In addition to design, the development and packaging has to be in India by Indian entity". Will there be an exception made in such a circumstance?**	This will be reveiewed on case to case basis and a waiver may be provided.

	3	**RFP Page #- Section- Sub-section: 9 – 6 – (e): Minimum Indicated Broad Specifications. While bidders are free to arrive at the optimum design/ configuration/ layout/ architecture of the SoCs to meet the market requirements and to enhance their marketability, it is mandatory for the SoCs to meet the Minimum Indicated Broad Specifications and features mentioned in the RFP.**	**Is it allowed to have variations of the specification for deployment? For example, if a user (especially in the commercial domain) requires a lower specification at a lower price point, would it be allowed to create such a reduced specification IC for this?**	As mentioned in the Section 6(e) (i.e. **Minimum Indicated Broad Specifications**) in Synopsis of the RFP, while bidders are free to arrive at the optimum design/ configuration/ layout/ architecture of the SoCs to meet the market requirements and to enhance their marketability, **it is mandatory for the SoCs to meet the Minimum Indicated Broad Specifications and features mentioned in the RFP.** Bidders are free to include **additional** features and functionalities to meet the chosen applications and end user's requirements. If the bidder wishes to develop variants of BSC-1 & BSC-2 to optimize the utility on more applications, they may do so **as long as they don't dilute the Minimum Indicated Broad Specifications, as mentioned in the RFP.**
	4	**RFP Page #- Section- Sub-section: 18 – 3: The Schedule of Work & Timelines of Stages. III Testing & Validation of Prototype BSC-1 & BSC-2 SoCs. Successful qualification of prototype SoCs.**	**It is not clear whether this involves a simulation, an FPGA-based prototype or an MPW tape-out of the silicon at this stage. Please clarify.**	As per Section 4(c) of Scope of work in the RFP (i.e. **Stage-III: Testing & Validation of Prototype BSC-1 & BSC-2**), Bidder shall undertake testing of the prototype SoCs to validate various IPs and security protocols used under his own arrangements and submit test reports & results to MeitY Technical Experts Committee for verification and validation. The RFP doesn't mandate the level of readiness of the Prototype to be made ready (i.e. Simulation model, FPGA-based prototype or MPW tape-out).

	5	**RFP Page #- Section- Sub-section: 73 – Appendix E – 1: MINIMUM INDICATED BROAD SPECIFICATIONS FOR BSC-1 SoC. 5 – High Speed Interface – PCI e Gen 3 Ethernet 10/100/1000 MAC:**	**The spec envisages a 300- 800 MHz primary core, but with both a 2-lane PCI- Express Gen 3.0 and gigabit Ethernet. These two requirements will lead to a mismatch between core and peripheral frequency. Please clarify whether gigabit ethernet is required, or 10/100 would be sufficient. Please also clarify whether the PCI Express is intended to be used as a host or as a peripheral (for example as a DAQ card in a PC).**	The specs of the SoC should be as per the minimum indicated broad specs. This will be reveiewed on case to case basis and a waiver may be provided.
	6	**RFP Page #- Section- Sub-section: 74 – Appendix E – 1: 5 – High Speed Interface - USB 3.x:**	**Please clarify whether the USB 3.x requirement here is for a host or device controller.**	USB Host and / Device ports may be provided as per the application requirement.
	7	**RFP Page #- Section- Sub-section: 75 – Appendix E – 2: MINIMUM INDICATED BROAD SPECIFICATIONS OF BSC-2 SoC. 1. CPU Core Complex – Pipelines - >= 6 Stage Dual Issue:**	**Is it allowed for BSC-2 to be a single-issue pipeline if the broad specification is otherwise met?**	This will be reveiewed on case to case basis and a waiver may be provided.

	8	**RFP Page #- Section- Sub-section: 75 – Appendix E – 2: 1. CPU Core Complex – DP FPU + Bit Manipulation + SIMD Extensions: Available:**	**The RISC-V opensource ISA has ratified the Vector extension for SIMD operations. Is this what is envisaged as SIMD?**	In case of RISC-V, Vector instructions are used instead of SIMD
	9	**RFP Page #- Section- Sub-section: 76 – Appendix E – 2: 8. Memory – Onchip NVM / FLASH: If application requires, Bidder may add the same:**	**Currently, there is no IP available for on-chip NVM/FLASH at geometries less than 28nm in most foundries. Will there be an exception made in case this is not available?**	May be decided as per requirements of application and availaibility of appropriate IP.

Invrese	**1**	**The key functionalities that these specifications lack are;** **1. Fault-tolerance** **2. Redundancy in core, functionality and peripherals** **3. Ability to fail-safe.** **BSC1 with a single core will make it difficult to certify products for many defence needs.** **Another point that needs to be considered is that most of the defence equipment worldwide are overwhelmingly on the 180/130nm, 90nm and 65/40 nm nodes. These nodes provide a much higher degree of noise and operational resilience. e.g. percentage of processors (made with 28 nm) that will experience electronmigration at 80 Deg C in 3 years is 5%. For 90 nm the same number is 0.08%. For 180 nm the figure is 0.0001%. So basically 1 in 20 devices using 28 nm WILL GO WONKY in 3 years. It is true there are ECCs etc., but how this will manifest is anyone's guess.**		May be decided as per requirements of application.